

FIG. 1

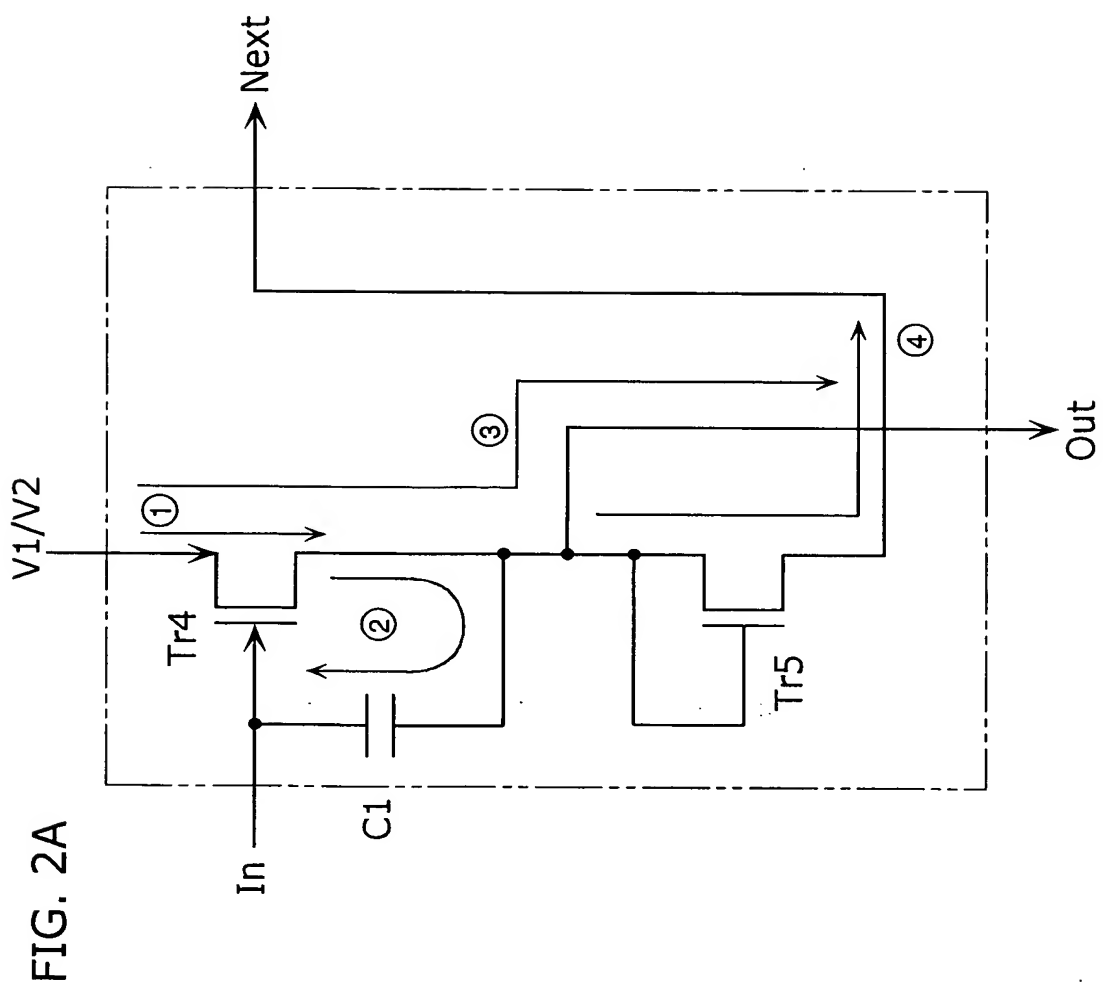


FIG. 2B

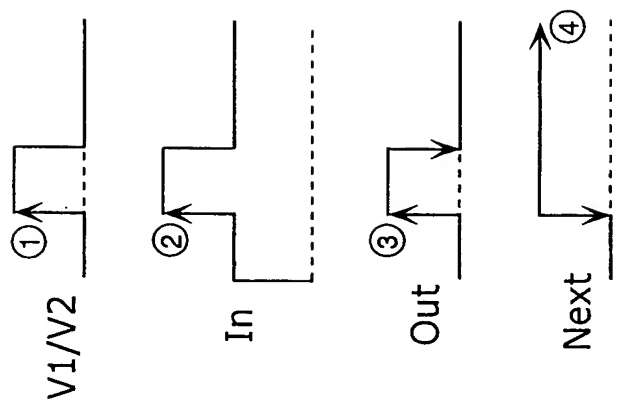


FIG. 3

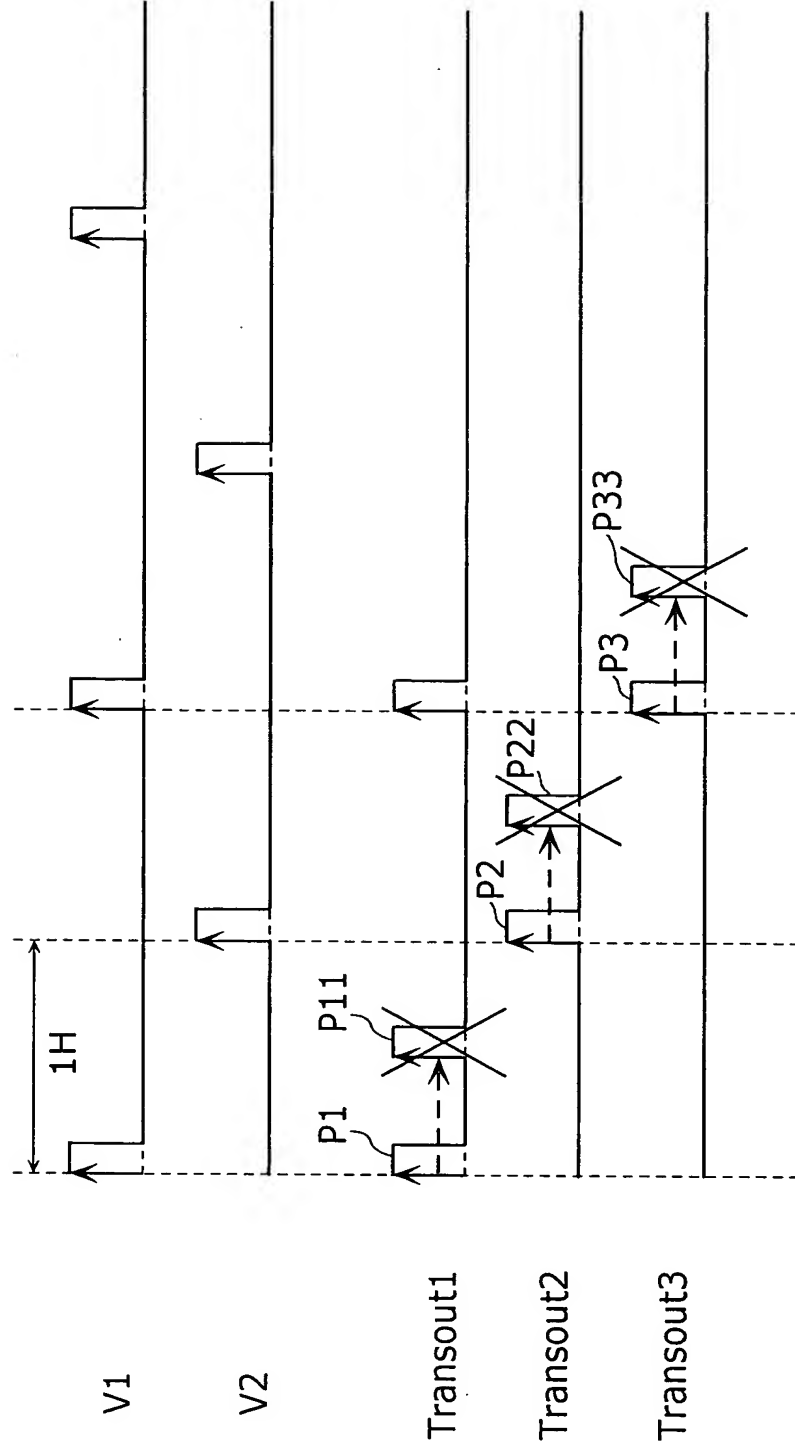
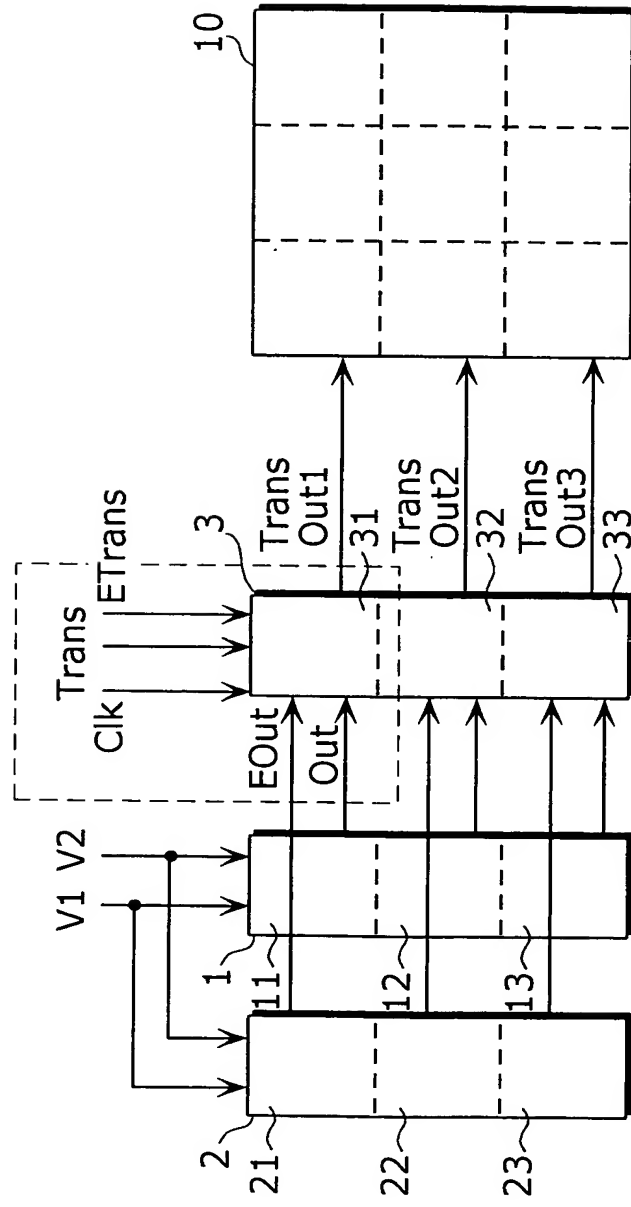


FIG. 4



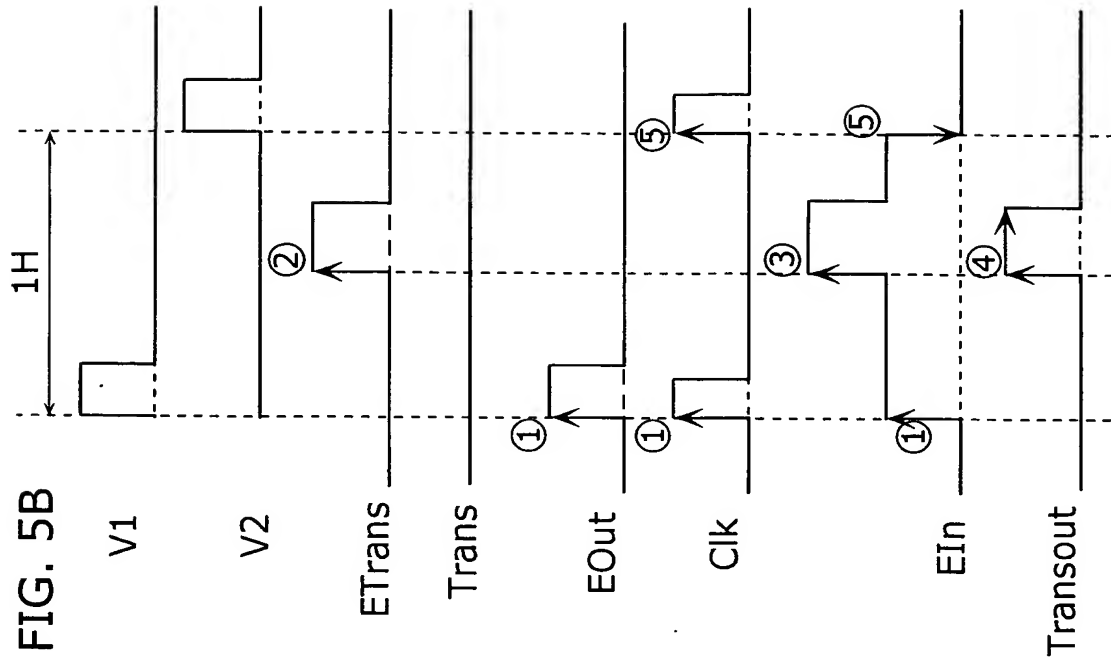
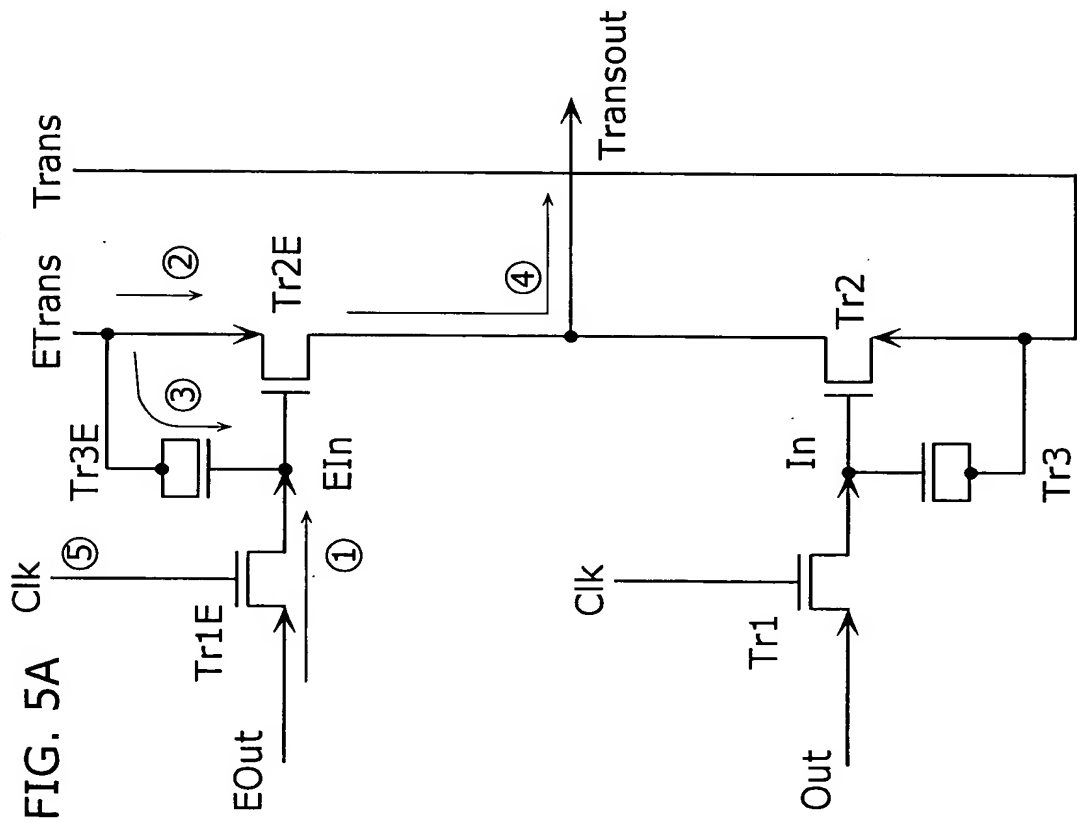


FIG. 6A

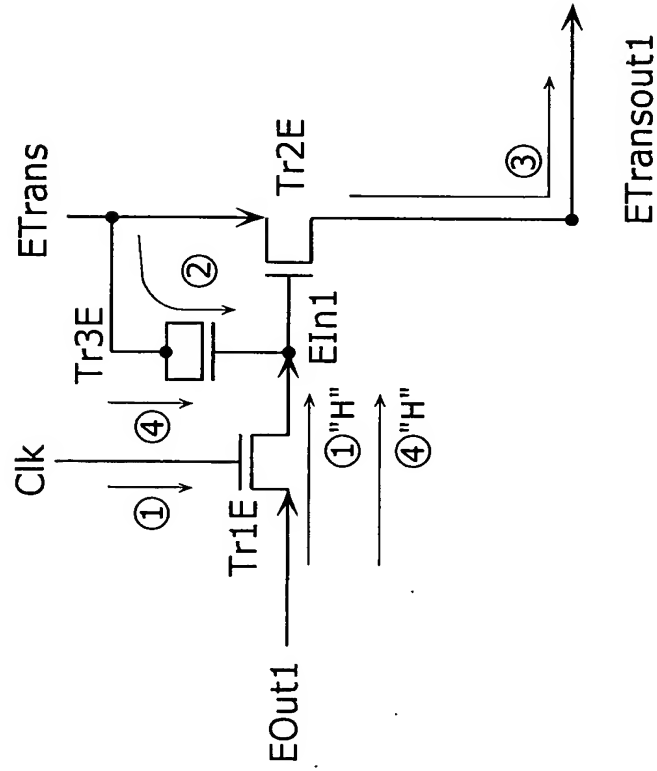
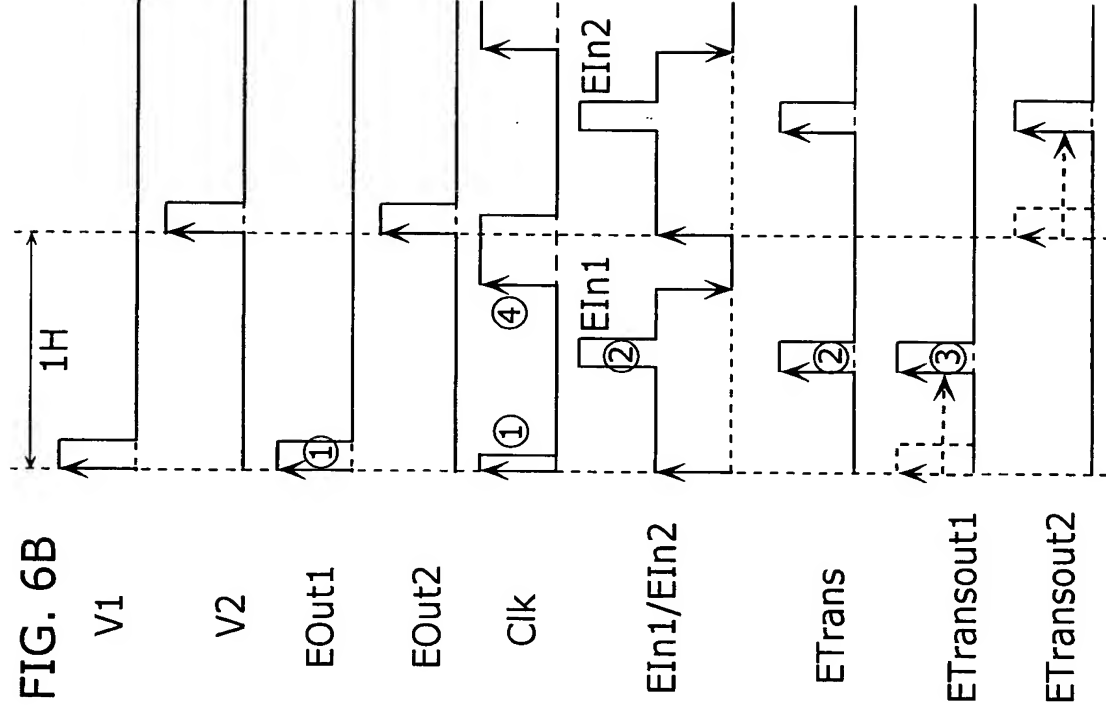


FIG. 6B



[illegible][illegible]

FIG. 8A

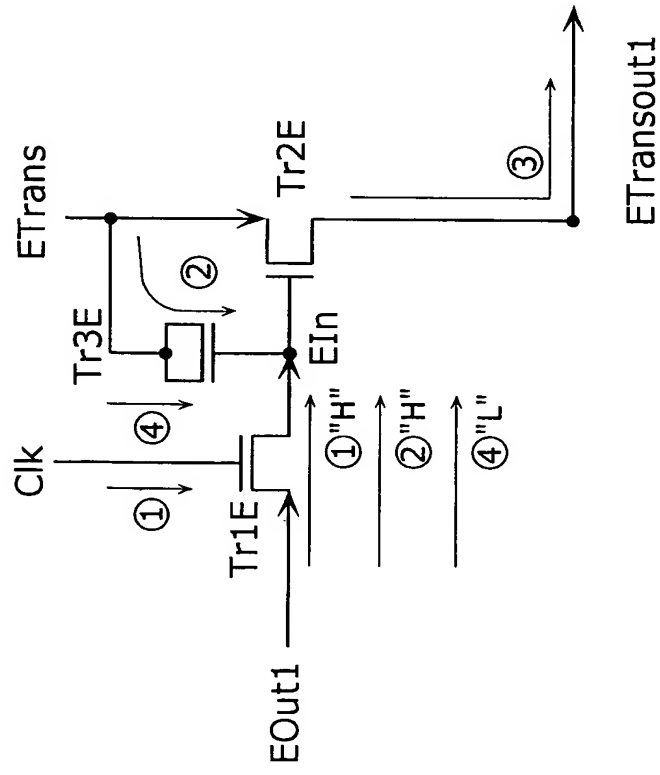
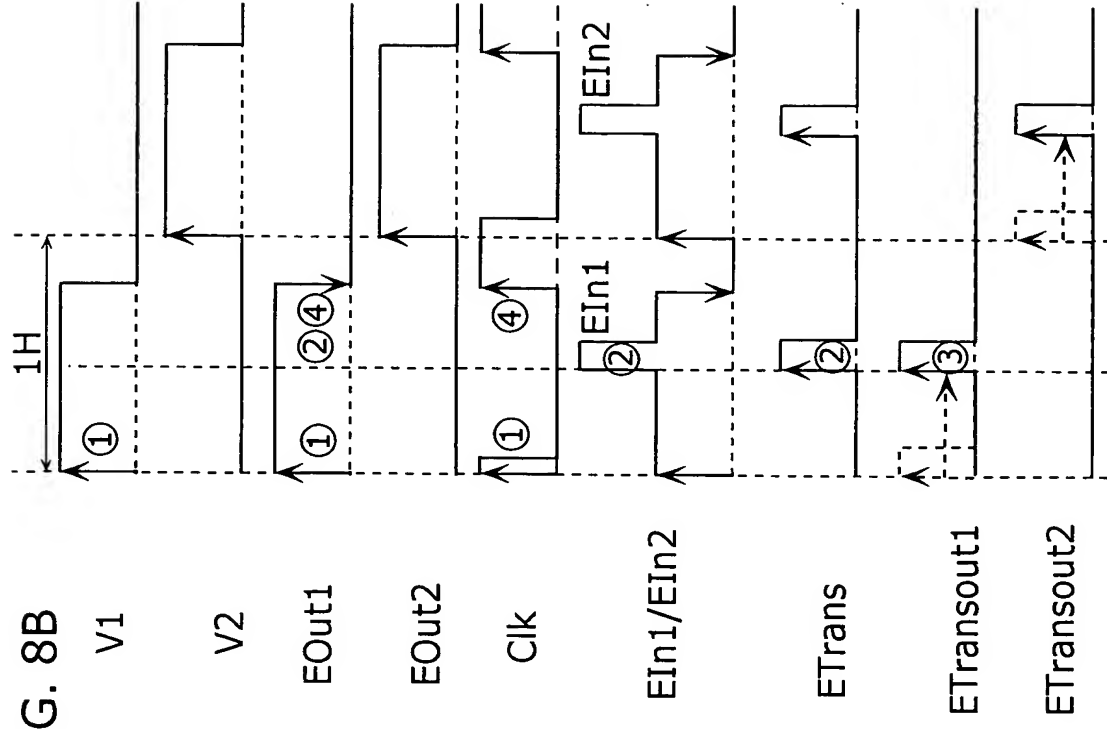


FIG. 8B



[illegible]

The diagram illustrates the timing and voltage levels for the EOUT1_EIn pin across four states:

- State 1:** CLK is high ("H"). The output voltage V is 2.8V.
- State 2:** CLK is high ("H"). The output voltage V is 1.8V.
- State 3:** CLK is high ("H"). The output voltage V is 4.5V.
- State 4:** CLK is high ("H"). The output voltage V is 0V.

The output is high-Z (High Impedance) when CLK is low ("L").

[illegible]

FIG. 10

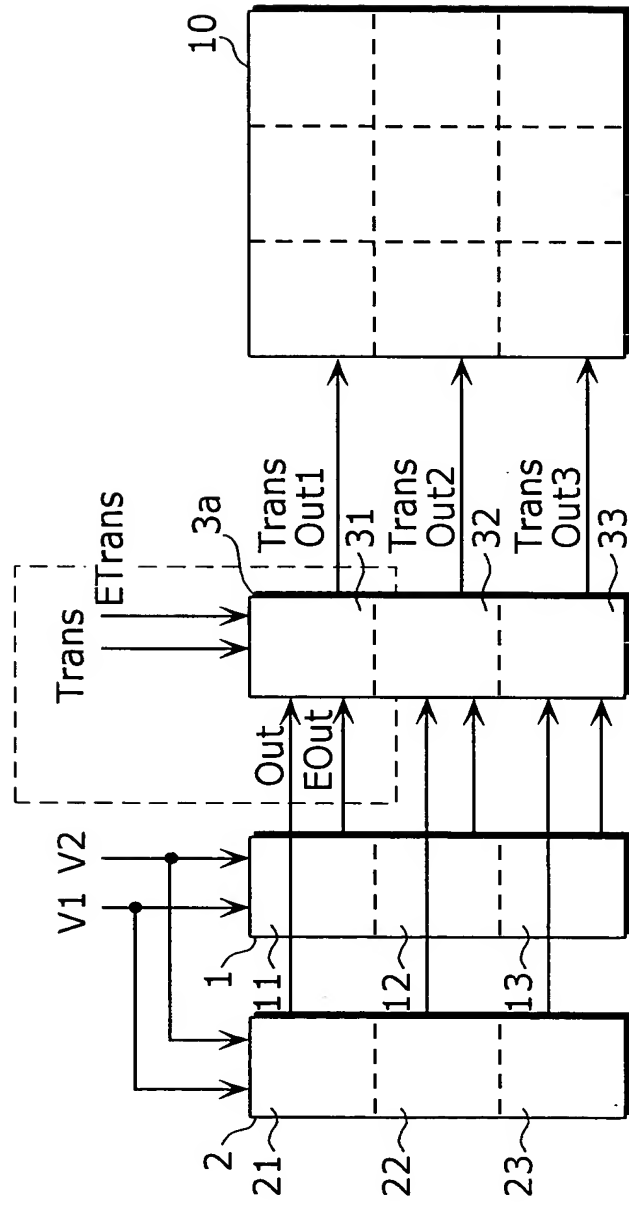
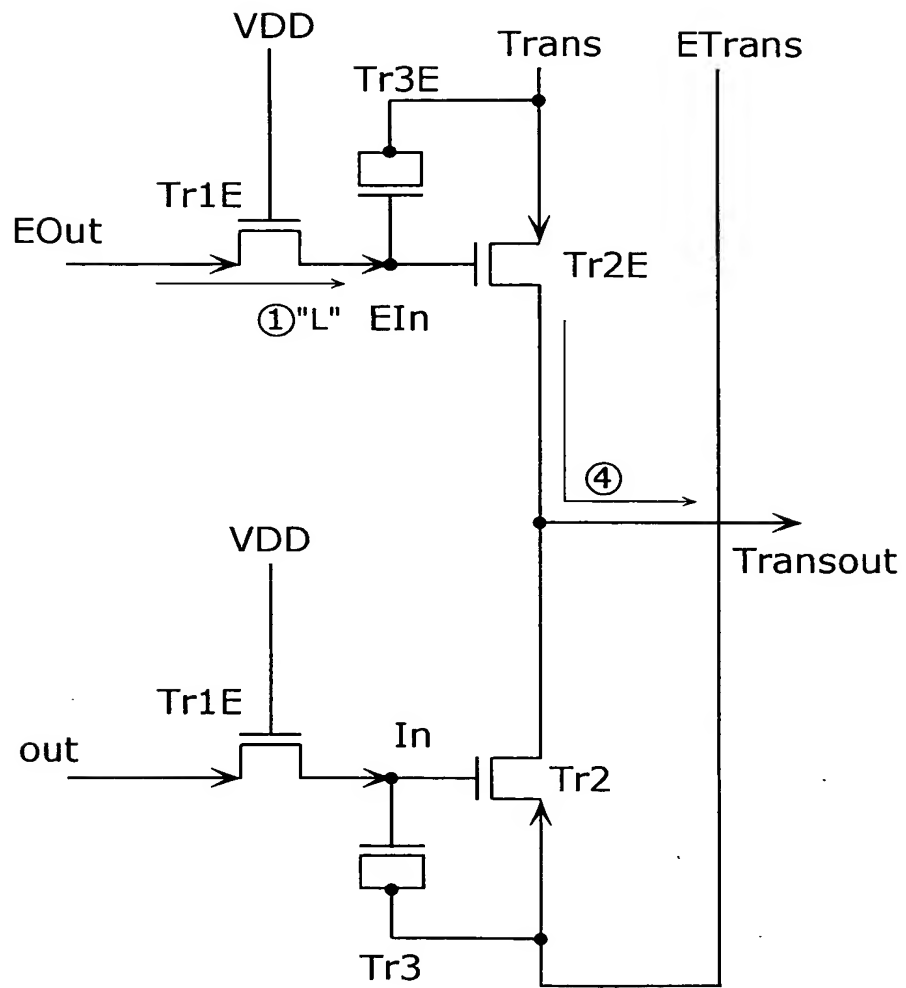


FIG. 11



VDD(DC) ETrans



FIG. 12B

